MODFET RELIABILITY STUDY

FINAL REPORT
MAY, 1988

Prepared by:
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Prepared for:
Naval Research Laboratory
Washington, D.C. 20375-5000

Contract No. N00014-86-C-2547

varian

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The objective of this program was to assess the reliability of MMICs fabricated using MODFETs as the active elements by investigating the reliability and failure mechanisms of the individual components, i.e. MODFETs, thin film resistors and MIM capacitors.

A monolithic MODFET distributed amplifier with 11dB gain from 2 to 20GHz and mid-band noise figure of 3dB recently developed at Varian with the support of the Naval Research Laboratory (Contract N00014-86-C-2048) is an example of this type of MMIC (Figure 1.0.1). These MODFET-based MMICs provide excellent performance. However, there are special reasons for concern over the reliability of MODFETs because their operation depends on extremely abrupt changes in material composition and doping level and there were early reports of very low MTTF. Also, there was very little reliability data on the other MMIC components, i.e. the tantalum nitride thin film resistors and the silicon nitride MIM capacitors, at the time this program was started.

The approach was to perform initial step-stress tests to determine an upper limit to the operating range and then

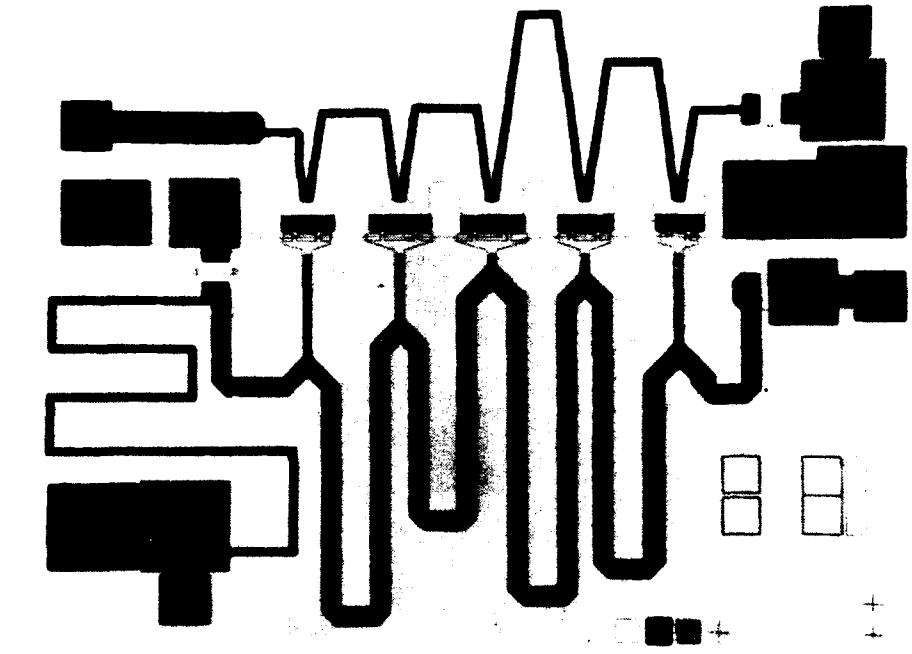


FIGURE 1.0.1

MMIC HEMT DISTRIBUTED AMPLIFIER CHIP

to perform high temperature storage, DC operating life tests and RF operating life tests, each at 3 temperatures to determine the median life and activation energy.

2.0 MODFET RELIABILITY STUDY

2.1 Introduction

The active element in the MMIC referred to in Section 1 is a MODFET (or HEMT - we shall use the terms interchangeably) with nominal 1/4 um gate length and active layers fabricated using MBE technology. The structure is shown in Figure 2.1.1. The intention of the program was to investigate the reliability of this device. However, at the beginning of the program a sufficient quantity of 1/4 um gate devices was not available and the reliability study was therefore started using nominal 1/2 um gate HEMTs. The principal differences between the two devices types are listed in Table 2.1.1. They will be referred to as 0.3 um HEMTs and 0.7 um HEMTs respectively. The devices were processed in the Varian Research Center and the Varian III-V Device Center respectively although the MBE for both lots was grown in the III-V Device Center.

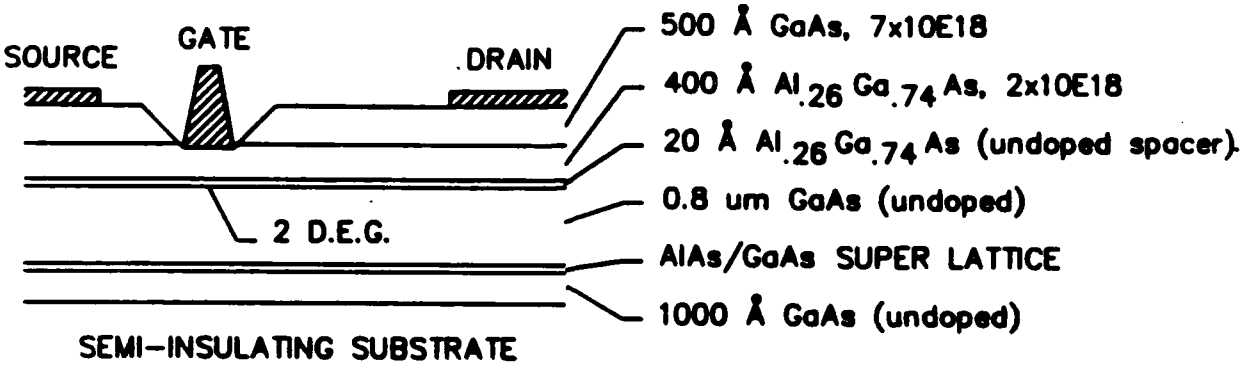


FIGURE 2.1.1

HEMT STRUCTURE

TABLE 2.1.1

Characteristics of 0.3 um-HEMT and 0.7 um HEMT

	0.3um HEMT	0.7um HEMT
Undoped AlGaAs Spacer (A)	20	50
Gate Length (um)	0.3	0.7
Gate Width (um)	150	285
Passivation	Si3N4	None
Idss (mA)	20	50
Vp (V)	0.6	0.7
Noise Figure (dB) (f=10 GHz)	0.9	1.2
Assoc. Gain (dB)	11.8	10.2

2.2 RF Burn-Out

The objective of the first tests was to determine the maximum RF input level. The units were each mounted in a microstrip test fixture, biased to the normal DC operating condition and the RF input level increased until the device failed. The results are summarized in Figure 2.2.1. RF burnout of the 0.3 um gate devices occurred at about 20dBm compared with 26dBm for the 0.7 um gate devices. The maximum RF input is roughly proportional to the gate area (the gate widths of the two device types are 150 and 285 um respectively). These burnout levels are over 10 dB above the linear operating range of the devices.

2.3 Automated Reliability Test System

The automated RF life test system developed under this program is shown schematically in Figure 2.3.1. Each unit is mounted in an individual microstrip test fixture provided with a heater, DC bias Ts and RF power source. The input power is adjusted by means of a PIN diode attenuator and monitored (via a 20dB coupler) to be sure there is no change in the RF input level during the

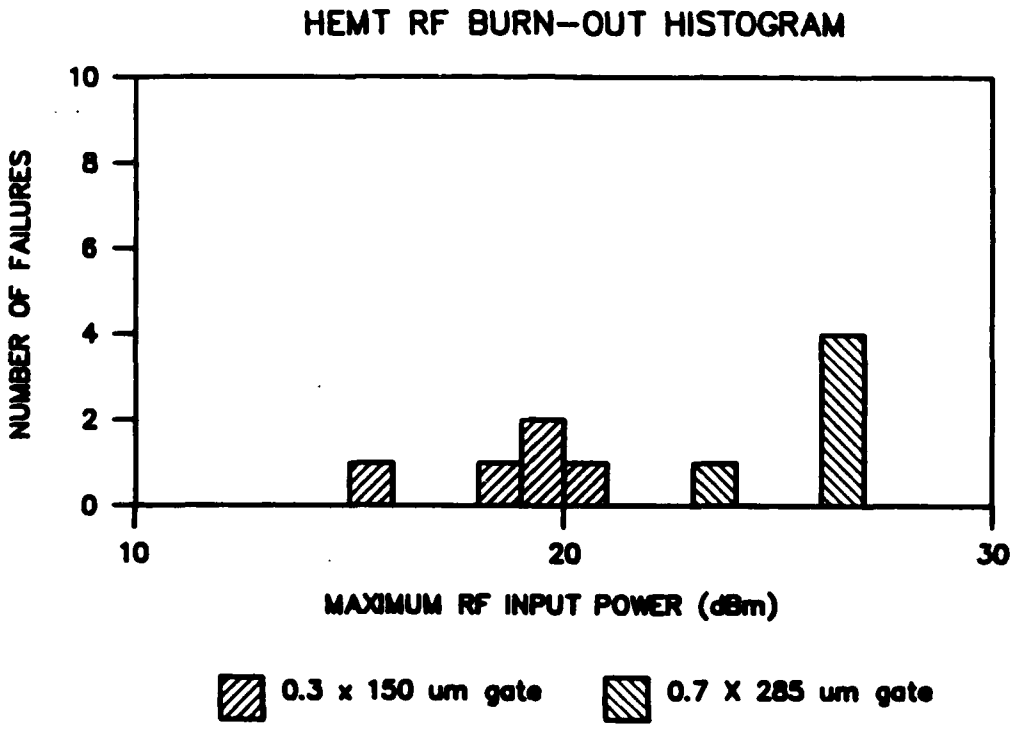


FIGURE 2.2.1

HISTOGRAM OF RF BURN-OUT LEVEL

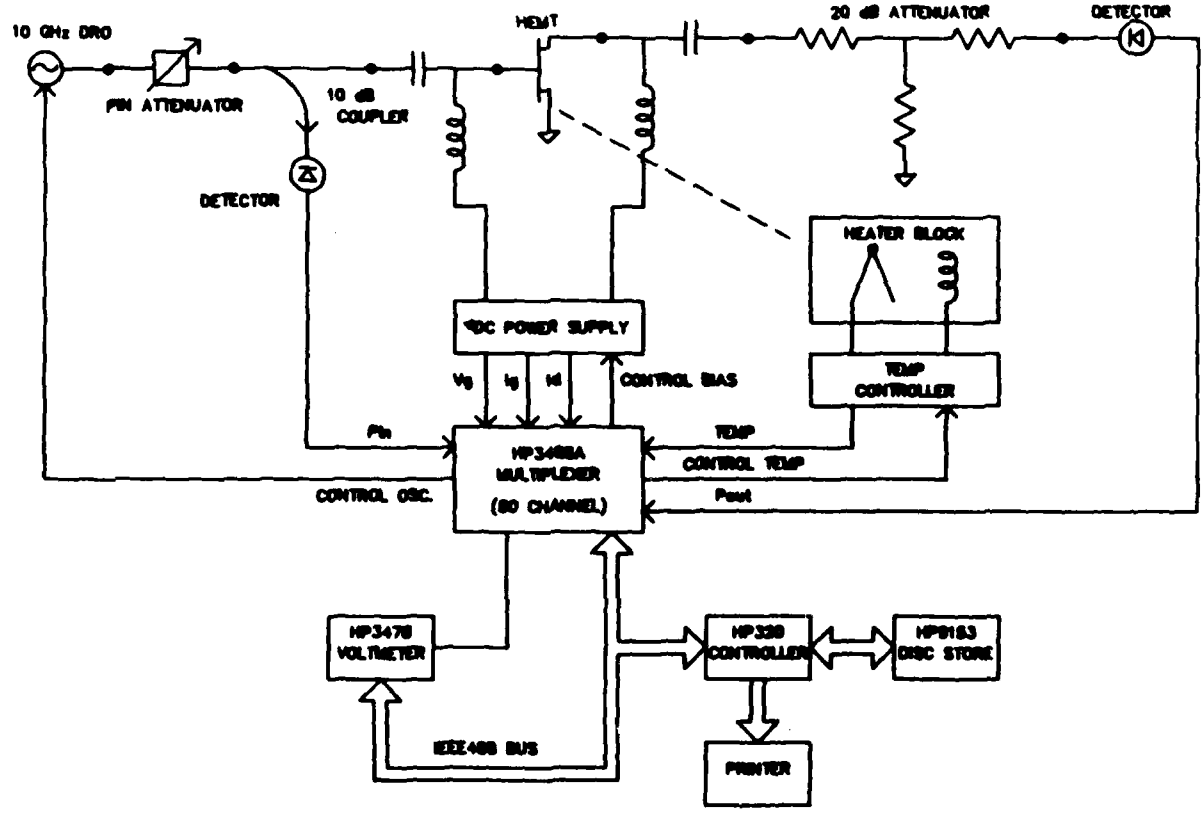


FIGURE 2.3.1

AUTOMATED LIFE TEST SYSTEM (SCHEMATIC DIAGRAM)

test. There are ten sites which are individually controlled and periodically monitored. When a unit exhibits a predetermined change in any of the monitored parameters i.e. Id, Ig or Pout, it is automatically turned off and the time of failure recorded. The purpose is not only to record the time of failure but also to prevent runaway and catastrophic failure. The unit is thus preserved for meaningful failure analysis. A photograph of the system is shown in Figure 2.3.2.

Although initially designed specifically for RF life tests, the advantages of an automated life test system relative to the traditional methods quickly became evident and in the final stages of the program it was also used for DC operating life tests and even high temperature storage.

2.4 High Temperature Storage

High temperature storage tests were started at 150°C using the 0.7 um HEMT and no significant changes were observed within the first 200 hours. When the temperature was increased to 225°C changes in Idss, transconductance and threshold voltage were observed;

FIRGURE 2.3.2

AUTOMATED LIFE TEST SYSTEM (PHOTOGRAPH)

there was no significant increase in either gate leakage current or source resistance. For a typical unit Idss decreased by 15% and gm decreased by 3% after 1000 hours (Figures 2.4.1 and 2.4.2). Figure 2.4.3 shows typical DC characteristics of a unit before and after high temperature storage: in addition to a decrease in the peak value of gm there is a shift of the peak to a lower gate voltage and there is also a slight shift in the threshold voltage.

Subsequently, the 150°C tests were continued to over 10,000 hours (Figure 2.4.4 and 2.4.5) and the devices exhibited changes similar to those observed at the higher temperature.

For the purpose of estimating the MTTF, we have defined a failure as a change in Idss of 20%: it was estimated, on the basis of a simple device model that this would correspond to an increase in noise figure of about 0.1dB.

In Figure 2.4.6 the cumulative failures in the high temperature storage test at 225°C are plotted on a probability scale vs the logarithm of time to failure. It is seen that a log normal distribution with a median life of 1800 hours was obtained. When devices became

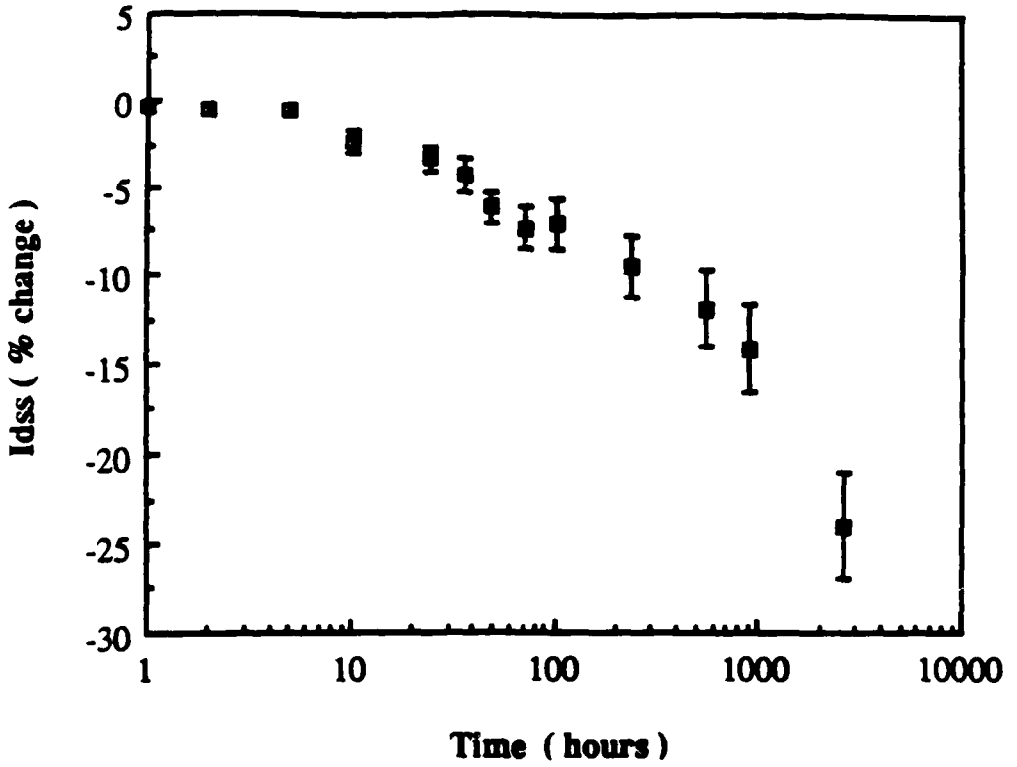


Figure 2.4.1 HIGH TEMPERATURE STORAGE: MEAN CHANGE IN Idss vs TIME AT 225°C (0.7 µm HEMT)

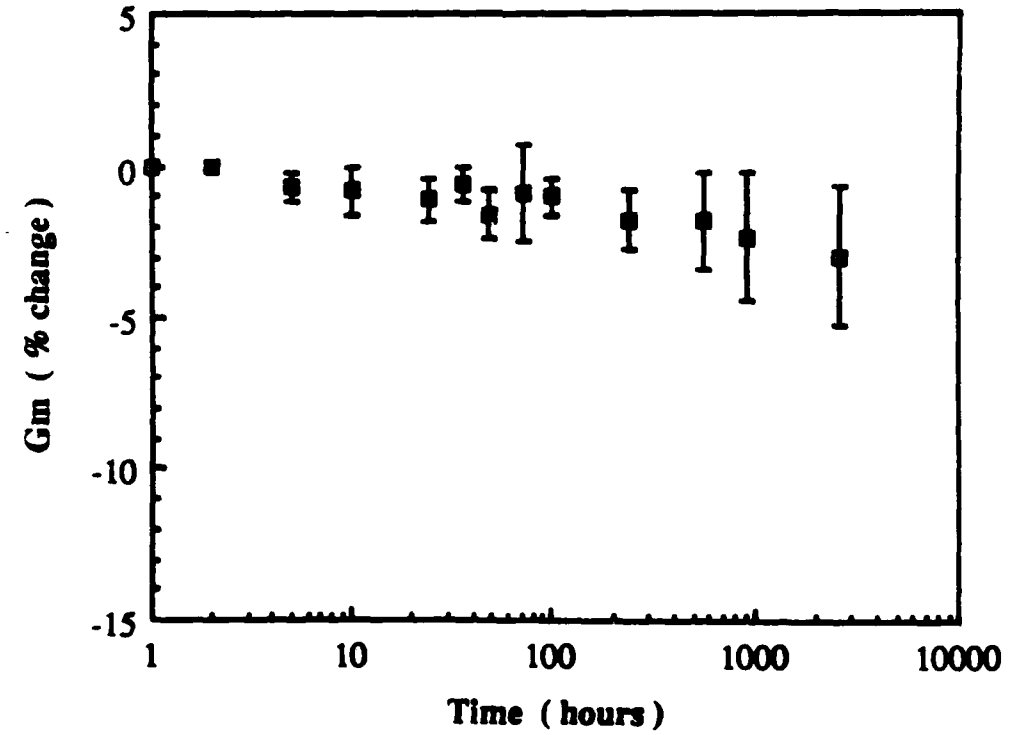


Figure 2.4.2 HIGH TEMPERATURE STORAGE: MEAN CHANGE IN gm vs TIME AT 225°C (0.7 µm HEMT)

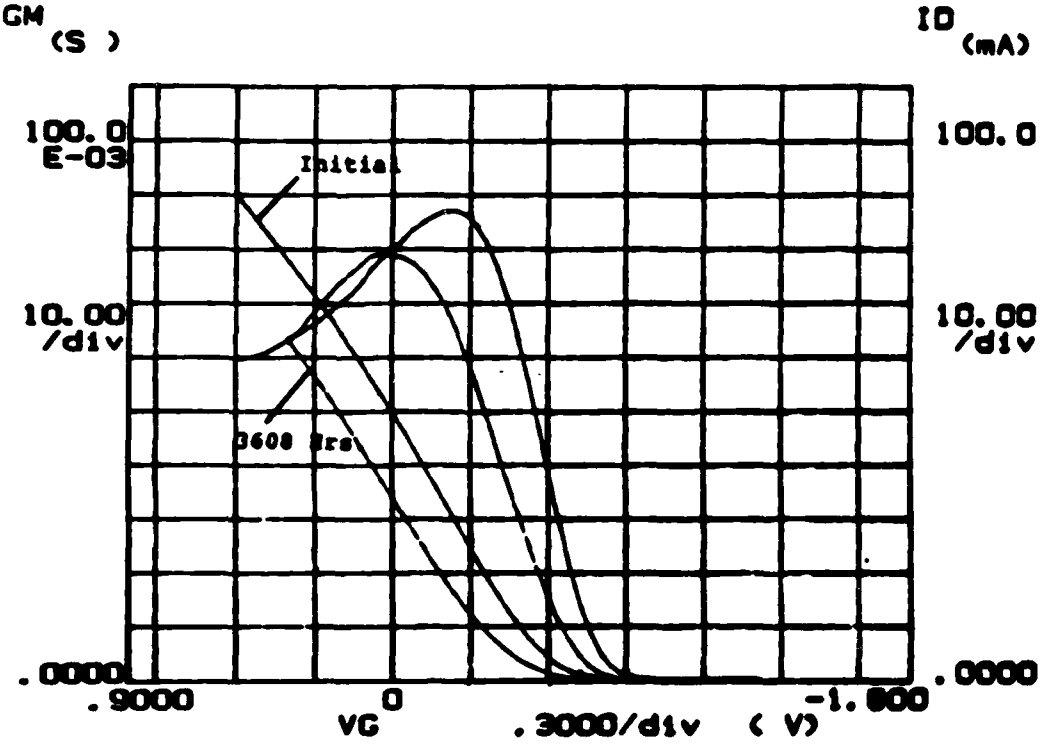


FIGURE 2.4.3

TYPICAL DC CHARACTERISTICS BEFORE AND AFTER HIGH TEMPERATURE STORAGE AT 225°C (0.7 μm HEMT)

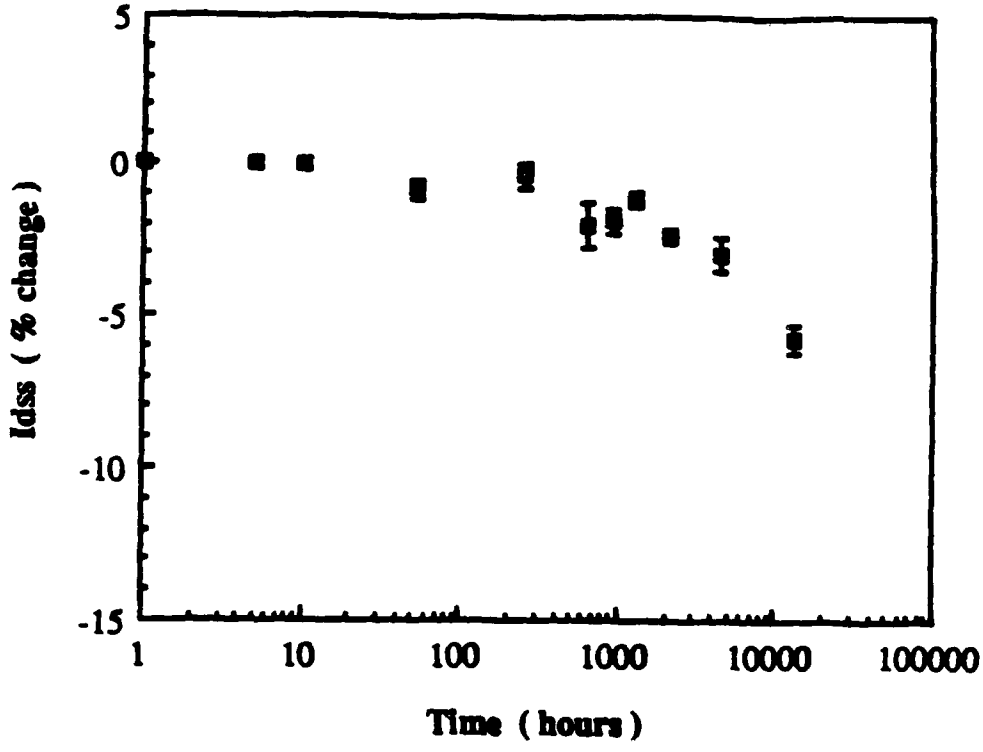


FIGURE 2.4.4 HIGH TEMPERATURE STORAGE: MEAN CHANGE IN Idss vs TIME AT 150°C (0.7 µm HEMT)

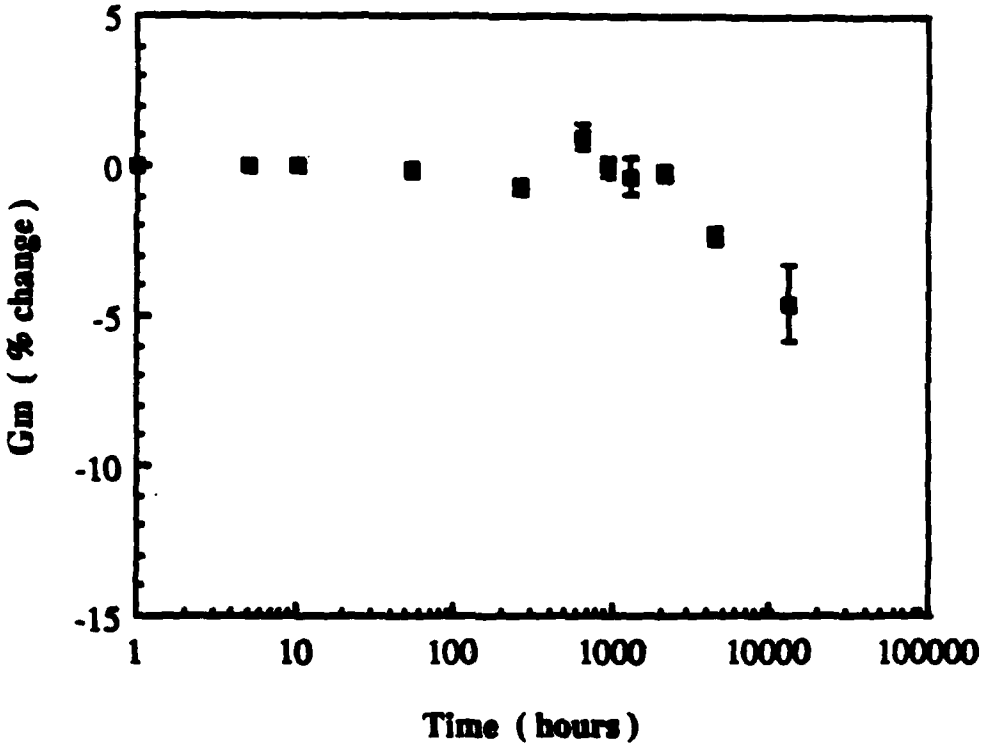


FIGURE 2.4.5 HIGH TEMPERATURE STORAGE: MEAN CHANGE IN gm vs TIME AT 150°C (0.7 µm HEMT)

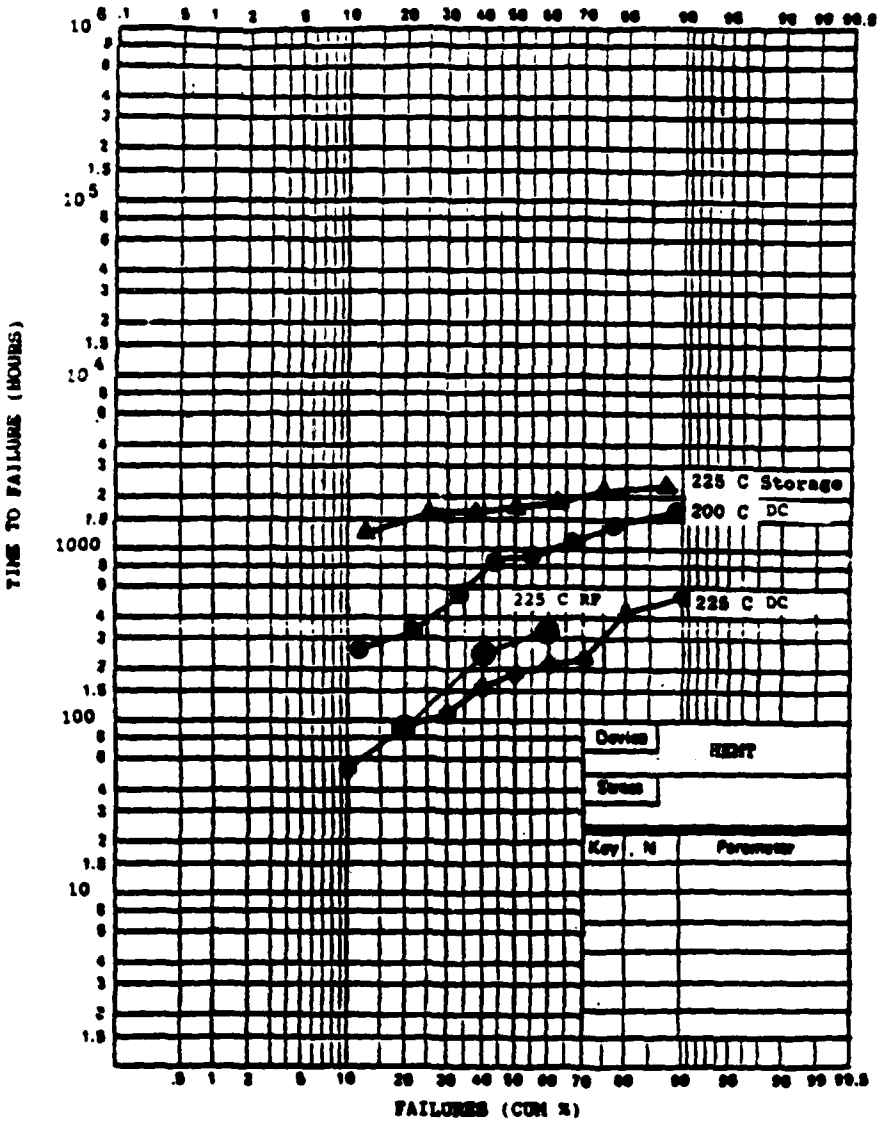


FIGURE 2.4.6

HIGH TEMPERATURE STORAGE, DC AND RF OPERATING LIFE TEST
FAILURE DISTRIBUTION FOR 0.7μm HEMT

available, high temperature storage tests of the 0.3 um HEMTs were also carried out at 225°C. In this case a median life of 35 hours was observed (compared with 1800 hours for the 0.7 um HEMT): the failure distribution is shown in Figure 2.4.7.

High temperature storage tests of the 0.3 um HEMT at 200°C and 250°C were carried out using the automated life test system. In this method, the devices were tested at temperature in comparison with the traditional method used for the test at 225°C, in which the devices were periodically removed from the oven for measurement. It was found that the change in room temperature Idss was greater than the change in Idss at the storage temperature. For example, the mean change in the magnitude of the room temperature I_{DSS} at the conclusion of the 250°C storage test was 36%. This explains the slight discrepancy between the 225°C storage test results and the computer-controlled storage test (200°C and 250°C) results. The failure distributions for these tests (where a failure is defined by a 20% change in Idss) are also included in Figure 2.4.7. A least-squares fit of the data at all these temperatures yields an activation energy of 1.0eV and a projected median life for the 0.3 um HEMT of 29,000 hours at a channel temperature of 120°C.

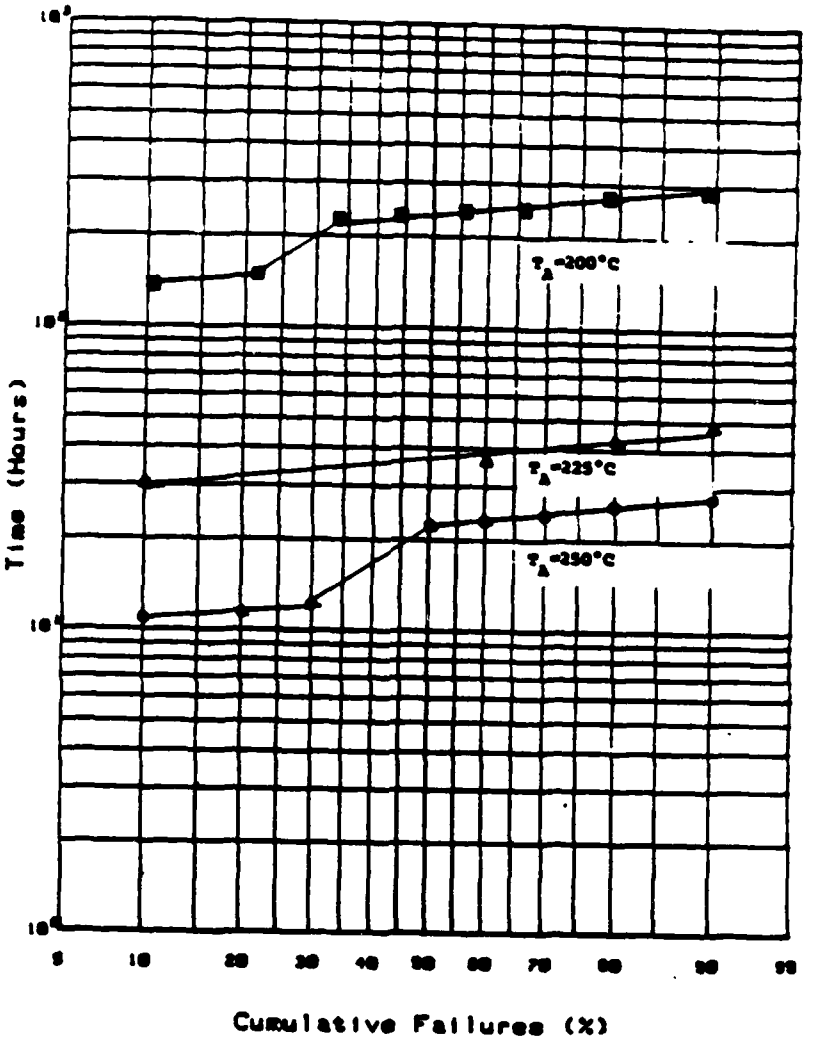


FIGURE 2.4.7

HIGH TEMPERATURE STORAGE FAILURE DISTRIBUTION
FOR 0.3 μm HEMT

The noise figure of the devices was measured before and after the 200°C and 250°C storage tests. The results are summarized in Table 2.4.1. Except for one unit there was no significant change in the noise figure within the limit of the measurement error.

2.5 DC Operating Life Tests

DC operating life tests of the 0.7 um HEMT were carried out at two temperatures, T_A=200°C and 225°C, using the traditional burn-in oven method prior to completion of the automatic life test system. The devices were periodically removed from the oven for testing. Again defining a failure as a 20% change in Idss the failure distributions are shown in Figure 2.4.6. The channel temperature of the devices was estimated to be 24°C above the oven temperature. Comparing the median life of 1800 hours for high temperature storage at 225°C with the median life of 950 hours for the DC operating life test at T_A=200°C (i.e. T_{CH}=224°C) there is evidence that the failure mechanism is accelerated by the DC electric field or current. Also, the standard deviation of the distribution of the failures is increased relative to the high temperature storage condition: this could be explained by the development of hot spots in the

TABLE 2.4.1

Summary of DC and RF Characteristics

Before and After High Temperature Storage

(0.3um HEMT)

	200 C		250 C	
	Before	After	Before	After
Idss (mA)	20.7±4.7	14.0±4.1	26.0±6.6	16.6±4.5
Vp (V)	0.61±0.12	0.48±0.11	0.75±0.20	0.58±0.16
Noise Figure	1.37±0.14	1.38±0.12	1.27±0.09	1.43±0.40*
Assoc. Gain (dB)	11.8±0.2	12.3±0.4	12.3±0.4	12.2±0.5

* 1.30±0.13 excluding one unit which increased to 2.6 dB.

DC operating condition. The 0.7 um HEMT DC operating life test data indicates an activation energy of 1.49 eV and projected median life of $9x10^6$ hours at a channel temperature of 120°C.

DC operating life tests of the 0.3 um HEMT were conducted at three temperatures (T_A=150, 175 and 200°C) using the automated test system. The distribution of failures obtained is shown in Figure 2.5.1. The operating conditions were Vds=4V, Id=15mA and the estimated channel temperatures were T_{CH}=185°C, 210°C and 235°C respectively. The failure mode observed was again a decrease in drain current and the failure criterion was defined as a 20% change in drain current. The samples at the two lower temperatures exhibit some early failures. A least squares fit of the data yields an activation energy of 1.1eV and a projected median life of 21000 hours at a channel temperature, T_{CH}=120°C.

2.6 RF Operating Life Test

The first RF operating life test (and the first use of the automated life test system) was conducted at T_A=225°C using 0.7 um HEMTs. The DC bias condition

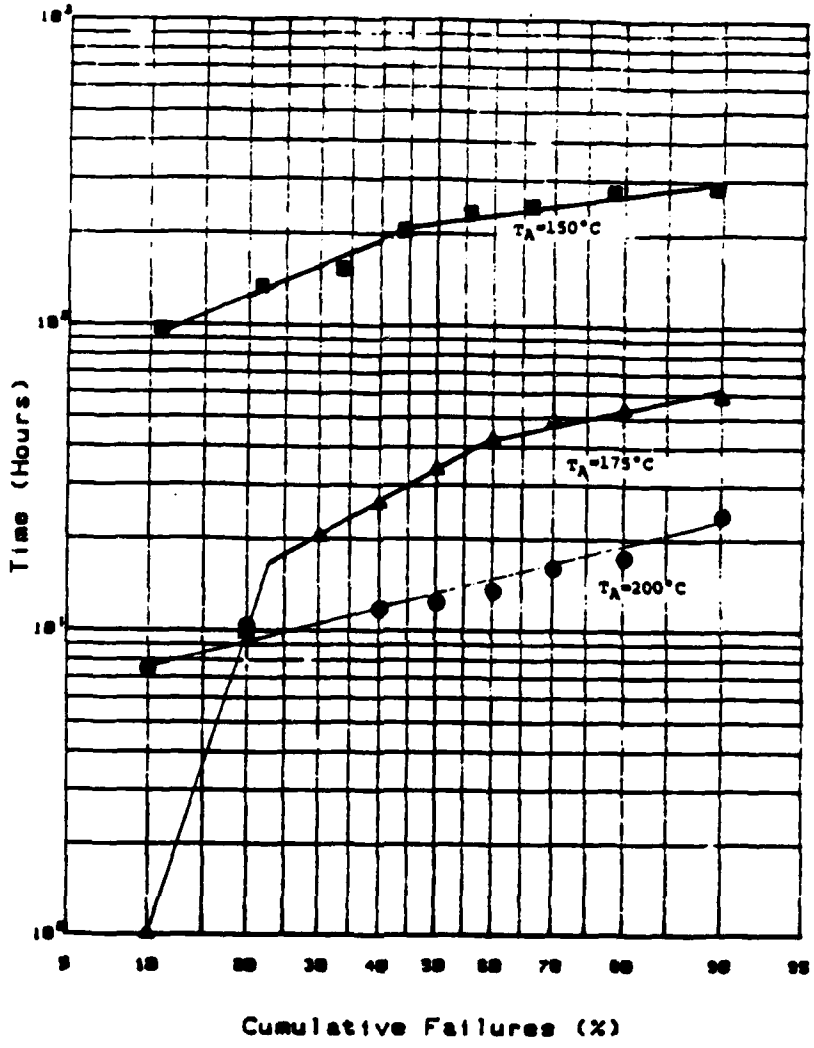


FIGURE 2.5.1

ACCELERATED DC LIFE TEST FAILURE DISTRIBUTIONS FOR 0.3 μm HEMT (Conditions V_{ds}=4 V, I_D=15 mA FAILURE: ΔI_d=20%)

was Vd=4V, Id=20mA and the RF level was adjusted (at room temperature) to obtain 1dB compression. The RF input level was typically 4-5dBm. The devices again exhibited a decrease in drain current and a failure was defined in terms of the change in drain current. The results are shown in Figure 2.4.6 for comparison with the high temperature storage and DC operating life tests. This was a test sample of only 5 units and the test was terminated when 3 units had failed. The difference between the DC and RF median life is therefore not considered statistically significant.

Accelerated RF life tests of 0.3 um HEMTs were conducted at three temperatures: T_A=175°C, 200°C and 225°C. The DC bias condition was Vds=4V, Id=15mA and the RF input level was typically 0dBm (for 1 dB compression). The estimated channel temperatures were T_{CH}=210°C, 235°C and 260°C. The failure mode observed was a decrease in drain current and a failure was defined by a 20% drop in Id. The failure distributions are shown in Figure 2.6.1. A least squares fit of the data yields an activation energy of 1.1eV and a projected median life of 26000 hours at a channel temperature T_{CH}=120°C. As in the case of the DC life tests a much shorter median life was observed for the 0.3 um HEMT than for the 0.7 um HEMT at the same channel temperature.

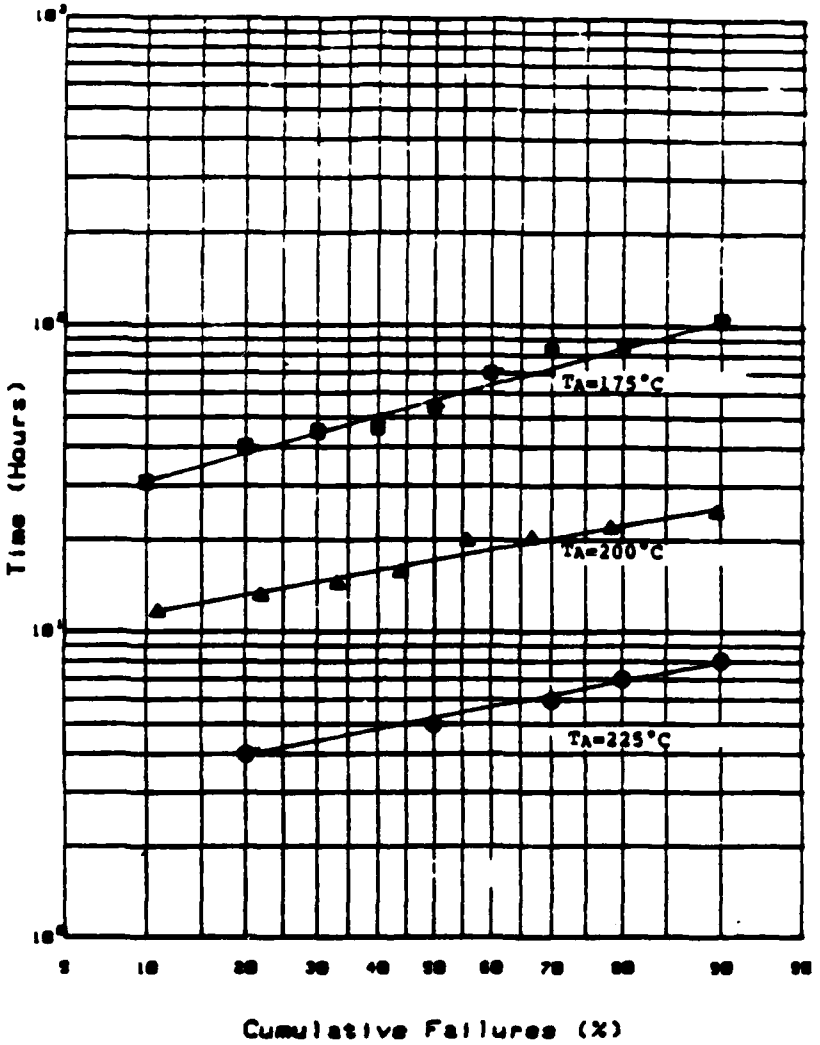


FIGURE 2.6.1

ACCELERATED RF LIFE TEST FAILURE DISTRIBUTIONS FOR 0.3 μm HEMT (CONDITIONS: V_{ds}=4 V, I_d=15 mA, PIN=0 dBm FAILURE: ΔI_d=20%)

Comparing the RF and DC life test results the median life is actually longer under RF drive. Possibly the average field is more uniform with RF compared to the DC case.

2.7 Summary of Results

The high temperature storage and accelerated life test (DC and RF) results are summarized in Figure 2.7.1. For tests which were carried out at 2 or more temperatures, the activation energy derived from a least squares fit of the data and the projected median life at T_{ch}=120°C are given in Table 2.7.1. The results show that the median life of the 0.7 um HEMT is 20-100 times longer than the median life of the 0.3 um HEMT in the temperature range at which the tests were conducted. The results also indicate that the activation energy for the failure mechanism in the 0.7 um HEMT is higher than that for the 0.3 um HEMT. However, this should be interpreted with caution because the 0.7 um HEMT result is based on data at only two temperatures (224°C and 249°C) compared with data over the range from 185°C to 260°C for the 0.3um HEMT.

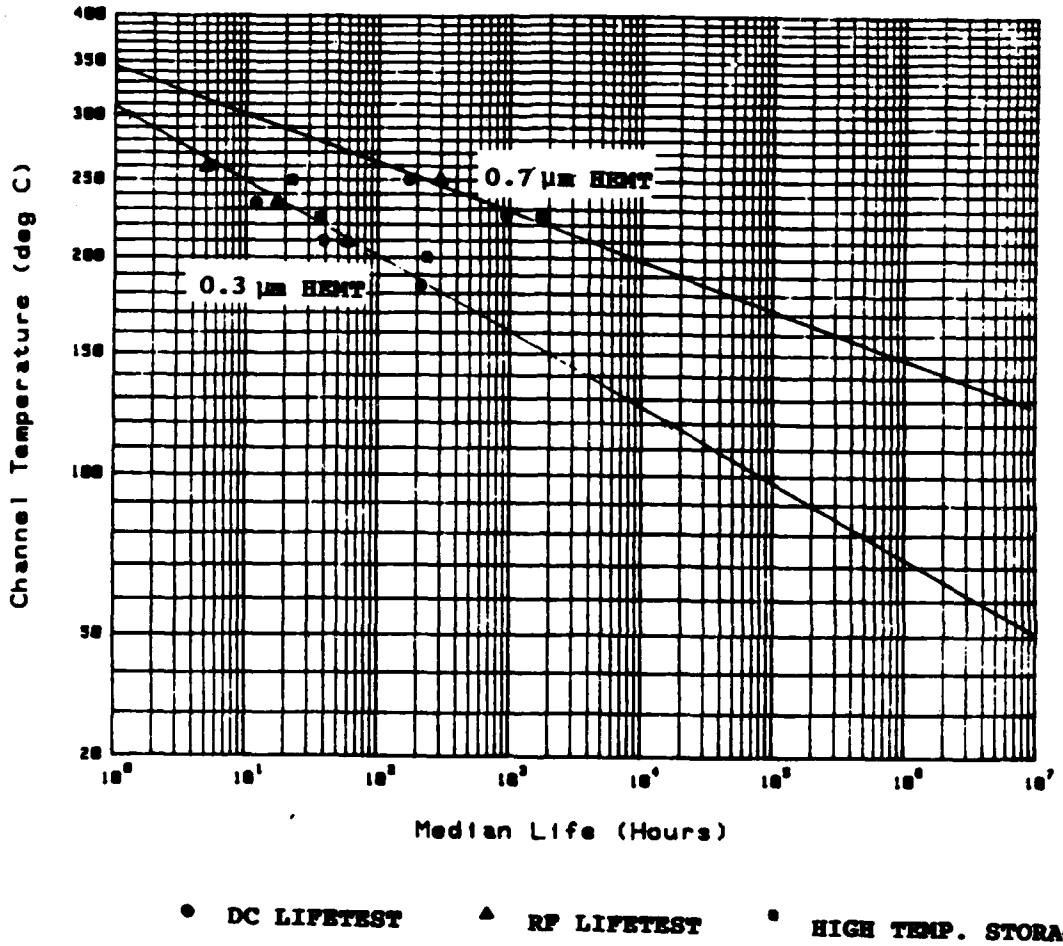


FIGURE 2.7.1

ARRHENIUS PLOTS OF MEDIAN LIFE FOR HIGH TEMPERATURE STORAGE, DC AND RF LIFE TESTS

TABLE 2.7.1

Summary of HEMT High Temperature
Storage, DC and RF Accelerated Life Test Results

Device Type	Type of Life Test	Activation Energy (eV)	Projected Median Life for Tch=120 C (hours)
0.7 um-Gate HEMT	DC Life Test	1.49	9.3×10^6
0.3 um-Gate HEMT	High Temp Storage	1.01	2.9×10^4
	DC Life Test	1.12	2.1×10^4
	RF Life Test	1.10	2.6×10^4

2.8 Discussion of Results

Possible mechanisms for changes in MODFET characteristics include:

- Redistribution of Si in the AlGaAs layer reducing the average doping level and the effective thickness of the undoped spacer layer, e.

- Out diffusion of Si, impurities or defects from the AlGaAs into the GaAs reducing carrier mobility and saturated velocity.

- Out-diffusion of Al from the AlGaAs into the GaAs reducing the conduction band discontinuity, ΔEc at the heterojunction.

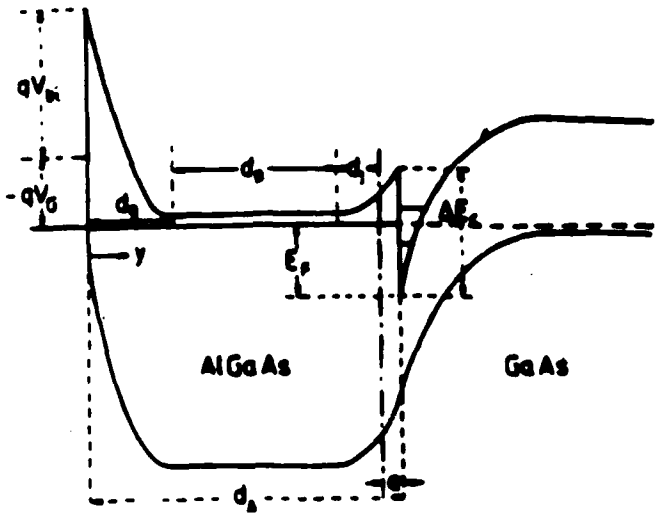
- Change in the Schottky barrier height.

- Migration of the Schottky metal-AlGaAs interface deeper into the AlGaAs reducing the effective AlGaAs thickness, d_a.

The effects of these changes have been modeled using the standard MODFET theory. For reference the MODFET energy

band diagram with a small negative gate bias and the expression for drain current, Id, are given in Figure 2.8.1.

It is seen immediately (Figure 2.8.2) that the redistribution of silicon into the spacer layer would cause an increase in drain current and threshold voltage which is contrary to the failure mode observed. Also the out-diffusion of Si (or other impurities) into the 2DEG region although reducing the drain current should have no significant effect on the threshold voltage (Figure 2.8.3). Reduction of the conduction band discontinuity at the heterojunction would reduce both the drain current and the threshold voltage (Figure 2.8.4) and is therefore a possible mechanism for the observed failure mode. The two mechanisms related to changes in the Schottky barrier could also explain the observed failure mode (Figures 2.8.5 and 2.8.6). The change in Schottky barrier height is unlikely: on GaAs the barrier height is relatively independent of the metal contact but this may not be true on AlGaAs. The penetration of the Schottky gate barrier into the AlGaAs is a more likely explanation of the observed failure mode. A similar failure mechanism has been reported for GaAs FETs (1,2). Because the AlGaAs layer is much more heavily doped than the normal FET



$$I_D = \frac{BV_C^2 \left\{ \left[1+2BR_S V_g' + (V_g'/V_C)^2 \right]^{\frac{1}{2}} - (1+BR_S V_g') \right\}}{(1-B^2 V_C^2 R_S^2)}$$

$$B = \frac{\varepsilon_A V_S Z}{(d_A + \Delta d) V_C}$$

$$V_g' = V_g - V_{off}$$

$$V_C = \varepsilon_C L_g$$

$$V_{off} = V_{bi} - \Delta E_c - \frac{q N_D}{2\varepsilon_A} (d_A - a)^2 + \Delta E_{FO}$$

FIGURE 2.8.1

MODFET ENERGY BAND DIAGRAM AND EXPRESSION FOR DRAIN CURRENT

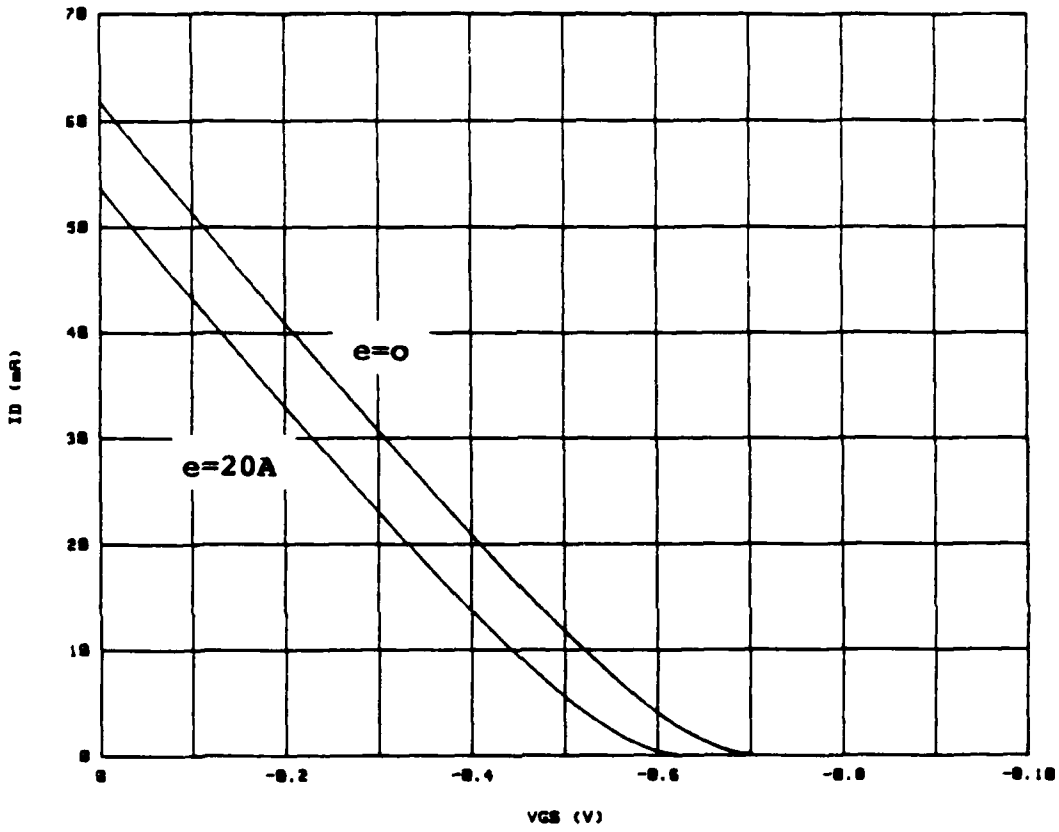


FIGURE 2.8.2

EFFECT OF AlGaAs SPACER THICKNESS ON DRAIN CHARACTERISTICS

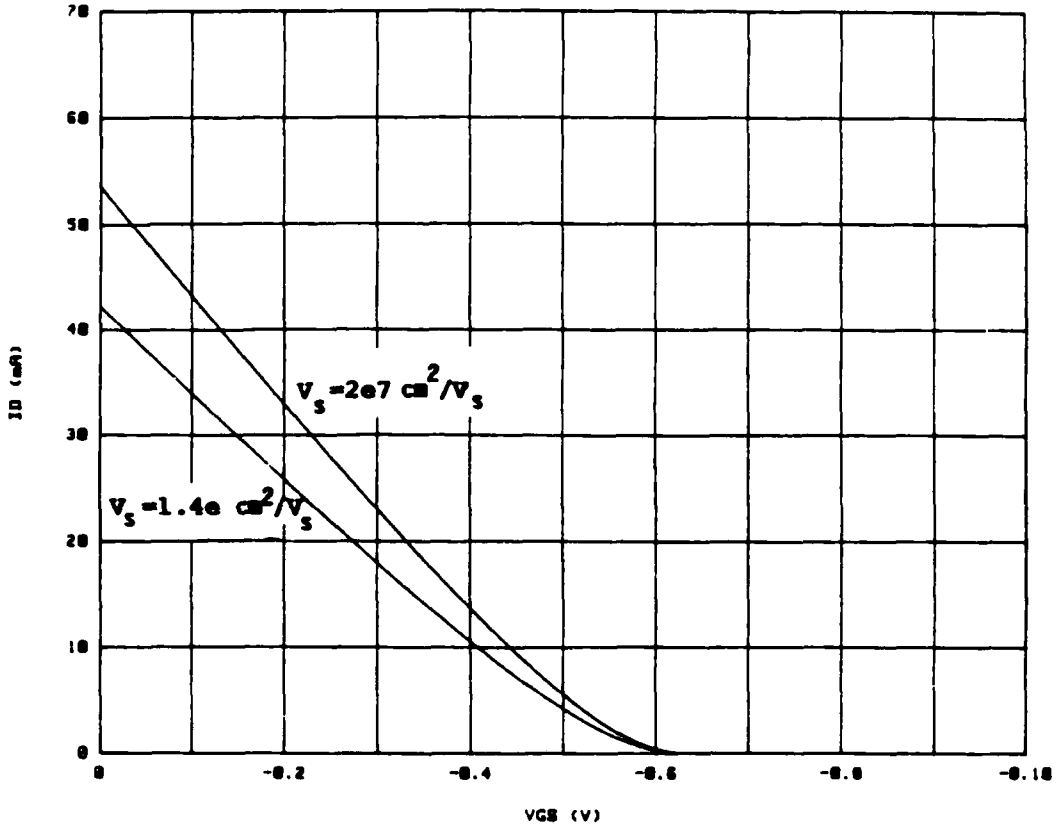


FIGURE 2.8.3

EFFECT OF SATURATED ELECTRON VELOCITY
v_s ON DRAIN CHARACTERISTICS

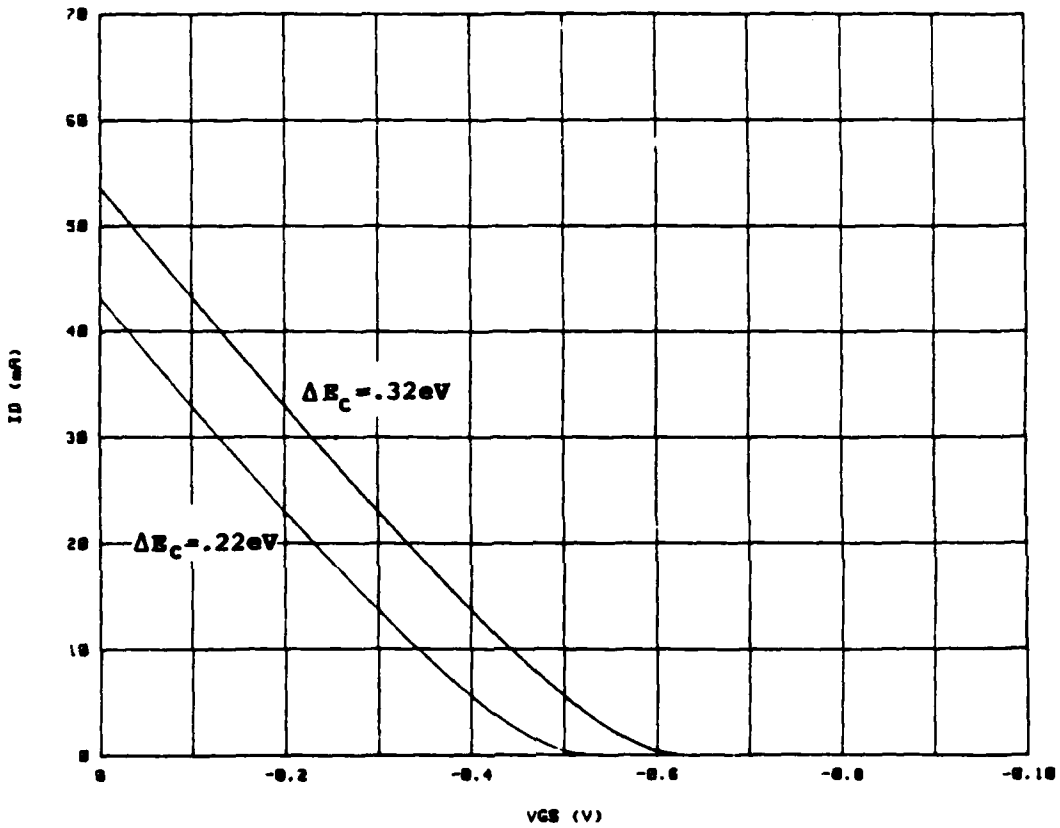


FIGURE 2.8.4

EFFECT OF CONDUCTION BAND DISCONTINUITY ΔE_c
ON DRAIN CHARACTERISTICS

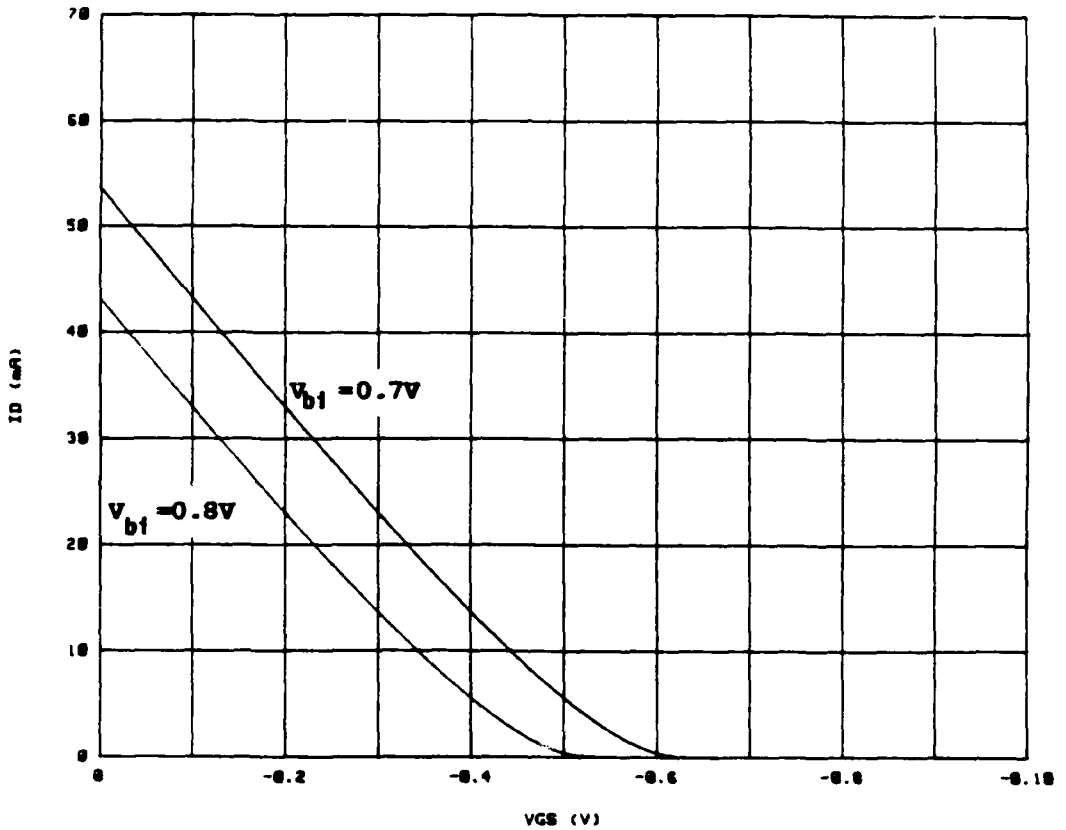


FIGURE 2.8.5

EFFECT OF SCHOTTKY BARRIER WEIGHT V_{bi}
ON DRAIN CHARACTERISTICS

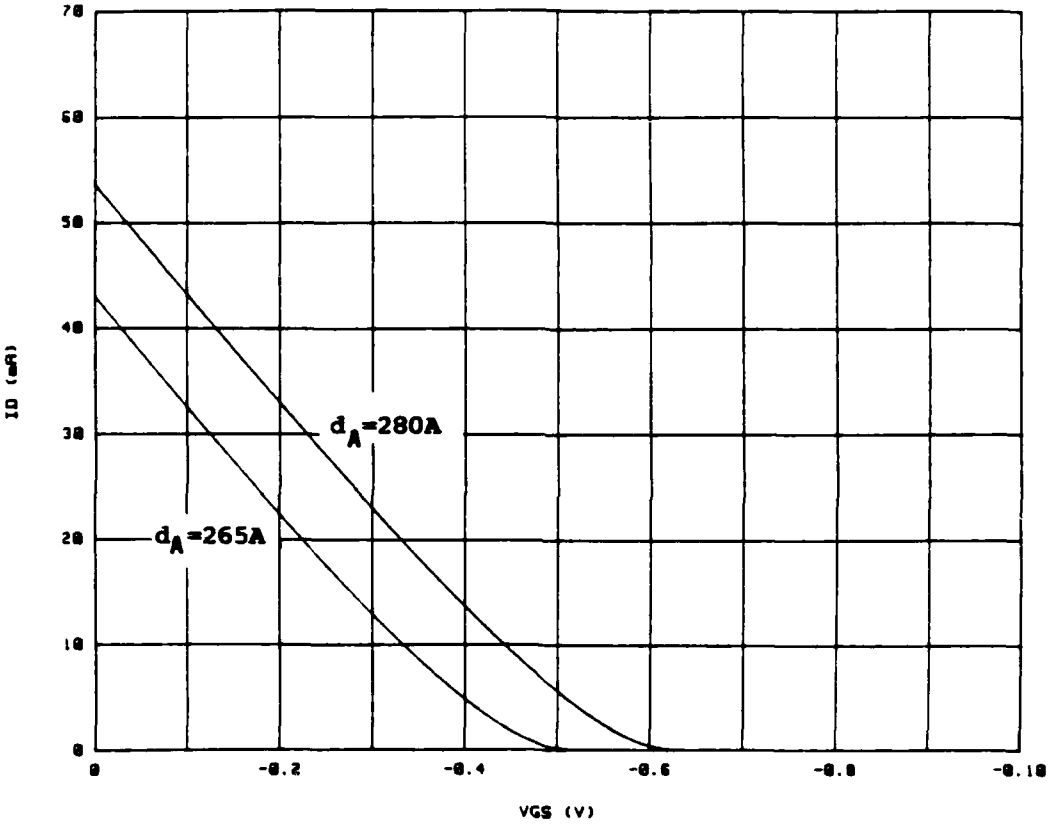


FIGURE 2.8.6

EFFECT ON AlGaAs THICKNESS d_A ON DRAIN CHARACTERISTICS

channel, the gate penetration required to produce the observed effect is only a few Angstrom units.

Thus there are two likely failure mechanisms for the observed MODFET degradation: Schottky barrier migration and heterojunction conduction band discontinuity reduction caused by aluminum migration.

Because two different activation energies have been observed for different device lots it is possible that both mechanisms may be involved.

Migration of gate metal and/or Al from the AlGaAs may be enhanced by defects. It is possible that the lower defect density in OMCVD material could explain the high reliability (no change in Idss after 300°C, 150 hour high temperature storage) reported for HEMTs built using OMCVD material (3).

The following experiments are proposed to distinguish between these possibilities and to identify the actual failure mechanism:

1. SIMS analysis of MODFET material with gate metallization on the n+ AlGaAs layer before and

after high temperature storage specifically looking for changes in the gate metal (Ti, Pt and Au) and Al profiles.

2. Evaluation, using the same testing procedure, of the reliability of FETs fabricated using the same process and gate metallization used for the MODFETs.

3. Evaluation of the reliability of MODFETs using OMCVD material.

3. MMIC CAPACITOR AND RESISTOR RELIABILITY STUDY

3.1 Introduction

The resistors and capacitors for this study were taken from the process control monitor (PCM) area of a completed MMIC wafer. The resistors have a nominal value of 50 Ohms and consist of a thin tantalum nitride film with gold contacts. The structure is shown in

Figure 3.1.1. The silicon nitride layer under the tantalum nitride is a barrier layer required to prevent interaction between the tantalum nitride and the GaAs surface. The MIM capacitors have the structure shown in Figure 3.1.2. The nominal capacitance per unit area is 300 pF/mm2 and the PCM capacitor has a nominal value of 3.0pF. For the purpose of the reliability study the resistors and capacitors were assembled in 4-lead T072 packages. In addition to resistance and capacitance measurements the leakage of the capacitors was characterized by measuring the voltage at which 1uA of leakage current was observed. Typically this breakdown voltage is >60V; attempts to measure at higher voltages usually result in catastrophic breakdown. This breakdown can occur either through the dielectric or through the substrate.

3.2 Determination of Maximum Operating Temperature

Both resistors and capacitors were step-stress tested to determine a maximum operating temperature, Tm. The DC operating condition was 40V for the capacitors and 25 mA for the resistors. The latter corresponds to the maximum rated current density of 5×10^3 A/cm2. The temperature was increased to 275°C in 25°C steps with 24 hour

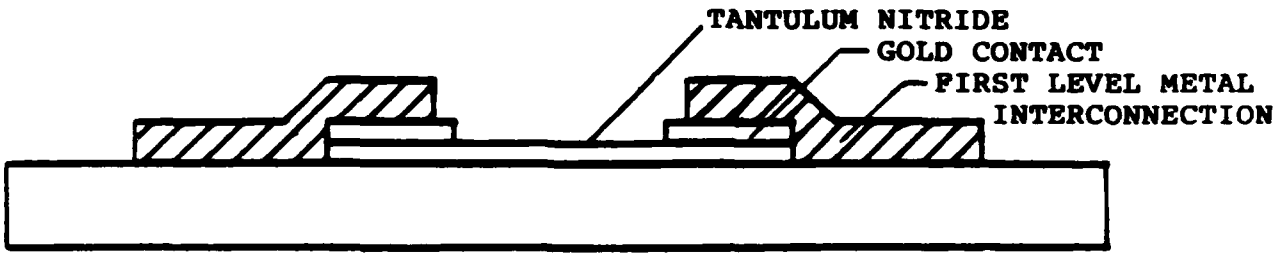


FIGURE 3.1.1

MMIC RESISTOR STRUCTURE

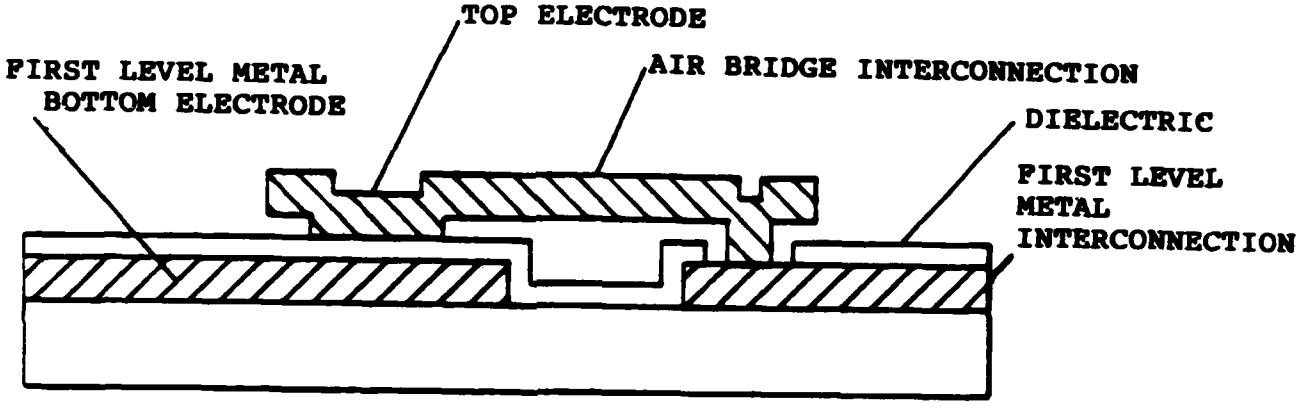


FIGURE 3.1.2

MMIC CAPACITOR STRUCTURE

dwell time at each temperature. The results are shown in Figure 3.2.1. A failure was defined for the capacitors as either a change in capacitance of $\pm$20% or breakdown voltage <40V and for the resistors as a change in resistance of $\pm$20%. Tm for capacitors is approximately 220°C, for resistors >275°C. The capacitors failed as a result of reduced breakdown voltage, not by a change in capacitance. No resistor failures were observed up to 275°C: the maximum change in resistance was $\leq$2%. To determine the cause of capacitor failure under DC bias, isolation test patterns, which consist of two closely spaced ohmic contacts to the GaAs substrate, were subjected to high temperature storage with DC voltage applied across the contacts: all of the units failed after 24 hours at 225°C. This strongly suggests that capacitor failures occur as a result of substrate rather than dielectric breakdown. A nitride layer between the lower electrode and the GaAs substrate as indicated in Figure 3.2.2 could provide a solution to this problem and would be simple to implement by minor changes in the existing process.

3.3 High Temperature Storage and DC Accelerated Life Tests

Based on the step-stress results a temperature T_A=210°C was selected for the high temperature storage

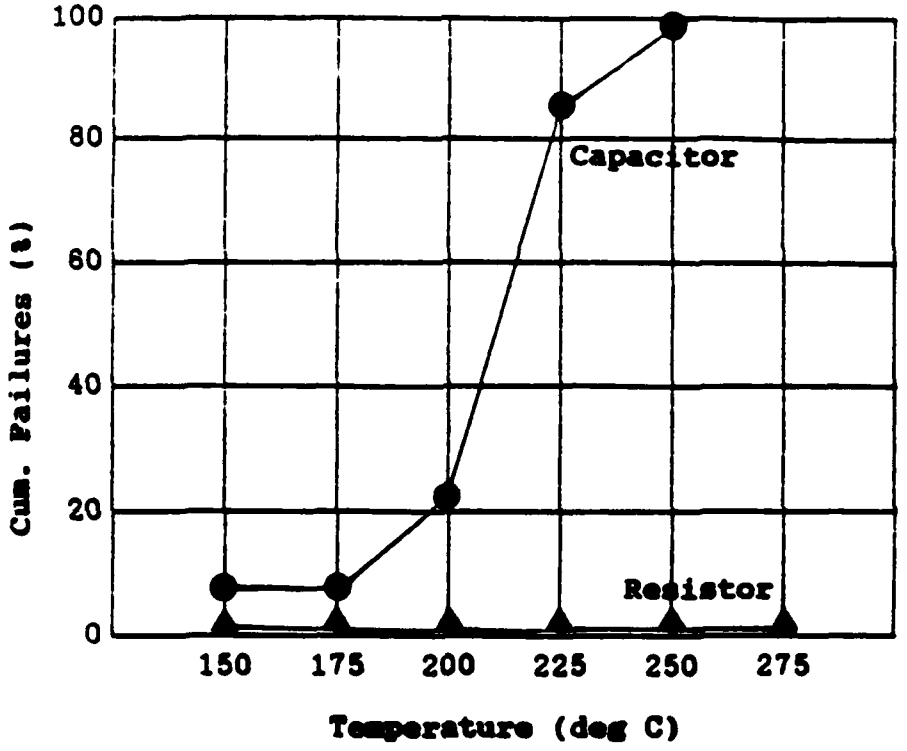


FIGURE 3.2.1

STEP-STRESS MAXIMUM TEMPERATURE DETERMINATION
FOR MMIC RESISTORS AND CAPACITORS

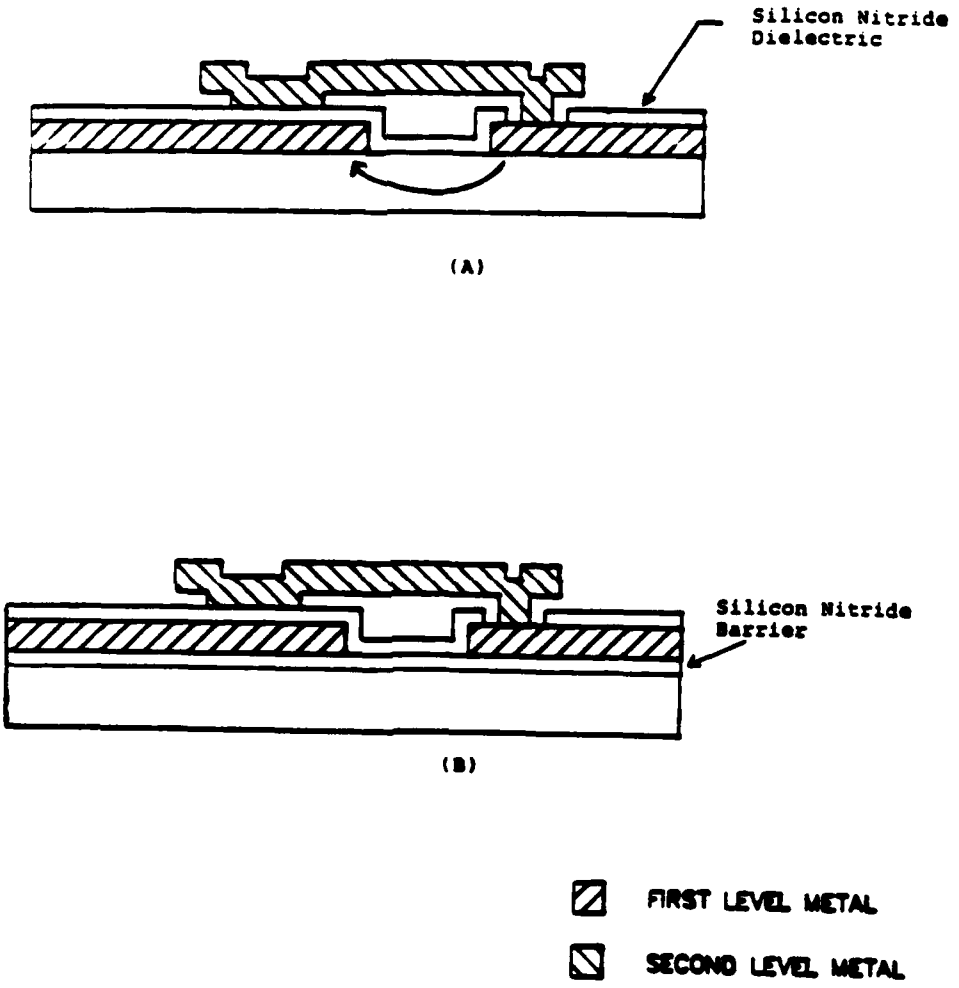


FIGURE 3.2.2

CAPACITOR CROSS SECTION (A) PRESENT STRUCTURE WITH POSSIBLE BREAKDOWN PATH INDICATED (B) PROPOSED STRUCTURE WITH SILICON NITRIDE BARRIER LAYER

and DC life tests. In the DC life tests the resistors were operated at the maximum rated current of 25 mA and 40V was applied to the capacitors. Both high temperature storage and DC life tests were continued to 1004 hours. The results are summarized as follows:

(1) Resistors

(a) High temperature storage

After 1004 hours high temperature storage the mean value of the 50 Ohm (nominal) resistors had increased from 52.3±0.6 Ohms to 53.5±0.6 Ohms an increase of 2.3%. The test included 11 units. The results are summarized in Figure 3.3.1.

(b) DC Operating Life Test

A sample of five resistors operating at the maximum rated current (25mA) increased in value by 6.2% after 1004 hours. (The test was started with 10 units but 5 were excluded because of fixture problems i.e. it was not certain that current was flowing in the resistors throughout the test). The estimated temperature of the TaN resistor film during the DC operating life test

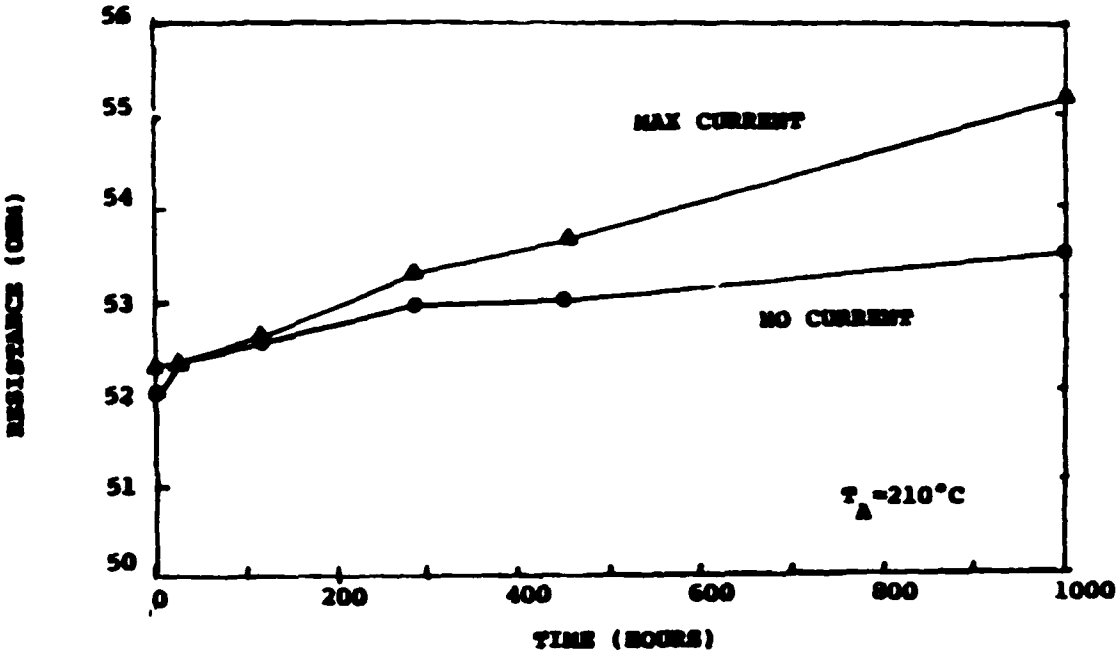


FIGURE 3.3.1

HIGH TEMPERATURE STORAGE AND DC OPERATING LIFE TEST RESULTS FOR MMIC TANTALUM NITRIDE RESISTORS

was 219°C. The resistor life tests are summarized in Figure 3.3.1.

(2) Capacitors

(a) High Temperature Storage

After 1004 hours high temperature storage the mean value of a sample of 9 3.0 pF (nominal) capacitors was unchanged. However, 2 units exhibited reduced breakdown voltage (30V and 40V respectively) after 454 hours. The initial breakdown voltage of all units and the final breakdown voltage of the remaining 7 units was >50V (the limit of the test).

(b) DC Operating Life Test

The DC operating life test was conducted with a sample of 9 units with 40V applied to the capacitors through a current-limiting resistor. Two units failed catastrophically (shorted) within the initial 28 hour period. The breakdown voltage of one unit had degraded to 20V; after 454 hours the remaining units maintained the initial breakdown voltage of >50V. There was no

measurable change in the capacitance of the 7 surviving units through the 1004 hour test.

4. SUMMARY

A reliability study of MODFET MMIC elements, namely MODFET devices, thin film tantalum nitride resistors and MIM capacitors with silicon nitride dielectric, has been completed with the following results:

- o High temperature storage induces changes in MODFET characteristics related to the sheet carrier concentration. (i.e. Idss, gm and Vp)

- o DC operating conditions accelerate these changes.

- o RF operation at normal signal levels does not increase the failure rate.

- o A significant difference in the median life was observed for two different lots.

- o Two failure mechanisms, i.e. Schottky gate barrier migration and heterojunction conduction band discontinuity lowering could account for the observed effects and recommendations for further work to

distinguish between these mechanisms have been proposed.

- o Tantalum nitride thin film resistors are stable at the maximum rated current at operating temperatures up to 210°C.

- o MIM capacitors exhibit a degradation of breakdown voltage when subjected to high temperature storage and DC life tests. The failure mechanism is substrate breakdown and a simple modification of the process has been proposed to eliminate this failure mechanism.

5. REFERENCES

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